REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and following remarks.

By the foregoing amendment, claims 1, 5, 8, 11, 14, 16 and 19 have been amended and claims 2, 3 and 9 have been canceled. No new matter is added. Thus, claims 1, 4-8 and 10-19 are currently pending in the application and subject to examination.

In the Office Action mailed April 26, 2005, the Examiner objected to claim 1 for informalities. Claim 1 has been amended responsive to this objection. If any additional amendment is necessary to overcome the objection, the Examiner is requested to contact the Applicants' undersigned representative.

The Examiner rejected claims 1-13 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,452,004 to Roberts (hereinafter, "Roberts"). Under 35 U.S.C. § 103(a), the Examiner rejected claims 14-16 as being unpatentable over Roberts in view of U.S. Patent No. 4,827,348 to Ernest et al. (hereinafter, "Ernest"), and claims 17-19 as being unpatentable over Roberts in view of Ernest and further in view of U.S. Patent No. 5,382,974 to Soeda et al. (hereinafter, "Soeda"). It is noted that claims 2, 3 and 9 have been canceled, and claims 1, 5, 8, 11, 14, 16 and 19 have been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

The Applicants respectfully submit that none of the cited prior art, nor combination thereof, discloses or suggests at least the combination of an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time,

and a switching circuit comprising a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line, as claimed in claim 1, as amended.

For at least this reason, the Applicants submit that claim 1, as amended, is allowable over the cited prior art. As claim 1 is allowable over the cited prior art, the Applicants submit that claims 4-8 and 10-13, which depend from allowable claim 1, are likewise allowable over the cited prior art.

Similarly to as discussed above with regard to claim 1, the Applicants submit that claim 14 is allowable over the cited prior art at least because none of the cited prior art, nor combination thereof, discloses or suggests at least the combination of an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time, and a switching circuit comprising a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line, as claimed in claim 14, as amended.

For at least this reason, the Applicants submit that claim 14 is allowable over the cited prior art. As claim 14 is allowable over the cited prior art, the Applicants submit that claims 15-19, which depend from allowable claim 14, are likewise allowable.

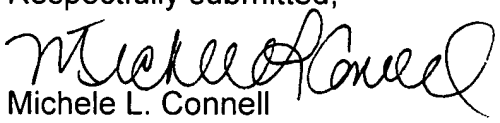
CONCLUSION

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing docket number **107317-00026.**

Respectfully submitted,



Michele L. Connell
Registration No. 52,763

Customer No. 004372
ARENT FOX PLLC
1050 Connecticut Ave., N.W., Suite 400
Washington, D.C. 20036-5339
Telephone No. (202) 857-6104
Facsimile No. (202) 857-6395
WC/MLC:elz